Chapter 4: Gate Direct Tunneling Current Model

As the gate oxide thickness is scaled down to 3nm and below, gate leakage current due to carrier direct tunneling becomes important. This tunneling happens between the gate and silicon beneath the gate oxide. The tunneling carriers can be either electrons or holes, or both, either from the conduction band or valence band, depending on (the type of the gate and) the bias regime.

In BSIM4, the gate tunneling current components include the tunneling current between gate and substrate (*Igb*), and the current between gate and channel (*Igc*), which is partitioned between the source and drain terminals by *Igc = Igcs + Igcd*. The third component happens between gate and source/drain diffusion regions (*Igs* and *Igd*). Figure 4-1 shows the schematic gate tunneling current flows.

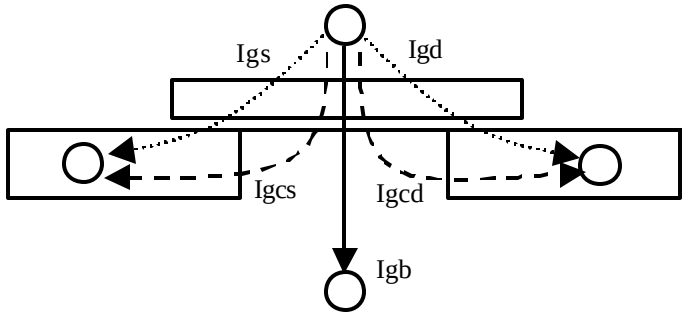

Figure 4-1. Shematic gate current components flowing between NMOST terminals in version.

4.1 Model selectors

Two global selectors are provided to turn on or off the tunneling components. ***igcMod*** = 1 turns on *Igc*, *Igs*, and *Igd*; ***igbMod*** = 1 turns on *Igb*. When the selectors are set to zero, no gate tunneling currents are modeled.

4.2 Voltage Across Oxide V_{ox}

The oxide voltage V_{ox} is written as $V_{ox} = V_{oxacc} + V_{oxdepinv}$ with

(4.2.1a)

$$V_{oxacc} = V_{fbzb} - V_{FBeff}$$

(4.2.1b)

$$V_{oxdepinv} = K_{1ox}\sqrt{\Phi_s} + V_{gsteff}$$

(4.2.1) is valid and continuous from accumulation through depletion to inversion. V_{fbzb} is the flat-band voltage calculated from zero-bias V_{th} by

(4.2.2)

$$V_{fbzb} = V_{th}\Big|_{zero V_{bs} and V_{ds}} - \Phi_s - K1\sqrt{\Phi_s}$$

and

(4.2.3)

$$V_{FBeff} = V_{fbzb} - 0.5\left[\left(V_{fbzb} - V_{gb} - 0.02\right) + \sqrt{\left(V_{fbzb} - V_{gb} - 0.02\right)^2 + 0.08V_{fbzb}}\right]$$

4.3 Equations for Tunneling Currents

4.3.1 Gate-to-Substrate Current (*Igb = Igbacc + Igbinv*)

Igbacc, determined by ECB (Electron tunneling from Conduction Band), is significant in accumulation and given by

(4.3.1)

$$Igbacc = W_{eff} L_{eff} \cdot A \cdot T_{oxRatio} \cdot V_{gb} \cdot V_{aux} \cdot \exp\left[-B \cdot TOXE\left(AIGBACC - BIGBACC \cdot V_{oxacc}\right) \cdot \left(1 + CIGBACC \cdot V_{oxacc}\right)\right]$$

where the physical constants A = 4.97232e-7 A/V^2, B = 7.45669e11 (g/F-s^2)$^{0.5}$, and

$$T_{oxRatio} = \left(\frac{TOXREF}{TOXE}\right)^{NTOX} \cdot \frac{1}{TOXE^2}$$

$$V_{aux} = NIGBACC \cdot v_t \cdot \log\left(1 + \exp\left(-\frac{V_{gb} - V_{fbzb}}{NIGBACC \cdot v_t}\right)\right)$$

Igbinv, determined by EVB (Electron tunneling from Valence Band), is significant in inversion and given by

(4.3.2)

$$Igbinv = W_{eff} L_{eff} \cdot A \cdot T_{oxRatio} \cdot V_{gb} \cdot V_{aux} \cdot \exp\left[-B \cdot TOXE\left(AIGBINV - BIGBINV \cdot V_{oxdepinv}\right) \cdot \left(1 + CIGBINV \cdot V_{oxdepinv}\right)\right]$$

where A = 3.75956e-7 A/V^2, B = 9.82222e11 (g/F-s^2)$^{0.5}$, and

$$V_{aux} = NIGBINV \cdot v_t \cdot \log\left(1 + \exp\left(\frac{V_{oxdepinv} - EIGBINV}{NIGBINV \cdot v_t}\right)\right)$$

4.3.2 Gate-to-Channel Current (*Igc*) and Gate-to-S/D (*Igs* and *Igd*)

Igc, determined by ECB for NMOS and HVB (Hole tunneling from Valence Band) for PMOS, is formulated as

(4.3.3)

$$Igc = W_{eff} L_{eff} \cdot A \cdot T_{oxRatio} \cdot V_{gse} \cdot V_{aux} \cdot \exp\left[-B \cdot TOXE\left(AIGC - BIGC \cdot V_{oxdepinv}\right) \cdot \left(1 + CIGC \cdot V_{oxdepinv}\right)\right]$$

where A = 4.97232 A/V^2 for NMOS and 3.42537 A/V^2 for PMOS, B = 7.45669e11 (g/F-s^2)$^{0.5}$ for NMOS and 1.16645e12 (g/F-s^2)$^{0.5}$ for PMOS, and

$$V_{aux} = NIGC \cdot v_t \cdot \log\left(1 + \exp\left(\frac{V_{gse} - VTH0}{NIGC \cdot v_t}\right)\right)$$

Igs* and *Igd -- *Igs* represents the gate tunneling current between the gate and the source diffusion region, while *Igd* represents the gate tunneling

current between the gate and the drain diffusion region. *Igs* and *Igd* are determined by ECB for NMOS and HVB for PMOS, respectively.

(4.3.4)

$$Igs = W_{eff} DLCIG \cdot A \cdot T_{oxRatioEdge} \cdot V_{gs} \cdot V_{gs}' \cdot \exp\left[-B \cdot TOXE \cdot POXEDGE \cdot \left(AIGSD - BIGSD \cdot V_{gs}'\right) \cdot \left(1 + CIGSD \cdot V_{gs}'\right)\right]$$

and

(4.3.5)

$$Igd = W_{eff} DLCIG \cdot A \cdot T_{oxRatioEdge} \cdot V_{gd} \cdot V_{gd}' \cdot \exp\left[-B \cdot TOXE \cdot POXEDGE \cdot \left(AIGSD - BIGSD \cdot V_{gd}'\right) \cdot \left(1 + CIGSD \cdot V_{gd}'\right)\right]$$

where A = 4.97232 A/V^2 for NMOS and 3.42537 A/V^2 for PMOS, B = 7.45669e11 (g/F-s^2)$^{0.5}$ for NMOS and 1.16645e12 (g/F-s^2)$^{0.5}$ for PMOS, and

$$T_{oxRatioEdge} = \left(\frac{TOXREF}{TOXE \cdot POXEDGE}\right)^{NTOX} \cdot \frac{1}{\left(TOXE \cdot POXEDGE\right)^2}$$

$$V_{gs}' = \sqrt{\left(V_{gs} - V_{fbsd}\right)^2 + 1.0e-4}$$

$$V_{gd}' = \sqrt{\left(V_{gd} - V_{fbsd}\right)^2 + 1.0e-4}$$

V_{fbsd} is the flat-band voltage between gate and S/D diffusions calculated as

If *NGATE* > 0.0

$$V_{fbsd} = \frac{k_B T}{q} \log\left(\frac{NGATE}{NSD}\right)$$

Else V_{fbsd} = 0.0.

4.3.3 Partition of *Igc*

To consider the drain bias effect, *Igc* is split into two components, *Igcs* and *Igcd*, that is *Igc* = *Igcs* + *Igcd*, and

(4.3.6)

$$Igcs = Igc \cdot \frac{PIGCD \cdot V_{ds} + \exp(-PIGCD \cdot V_{ds}) - 1 + 1.0e-4}{PIGCD^2 \cdot V_{ds}^{\ 2} + 2.0e-4}$$

and

(4.3.7)

$$Igcd = Igc \cdot \frac{1 - (PIGCD \cdot V_{ds} + 1) \cdot \exp(-PIGCD \cdot V_{ds}) + 1.0e-4}{PIGCD^2 \cdot V_{ds}^{\ 2} + 2.0e-4}$$

If the model parameter *PIGCD* is not specified, it is given by

(4.3.8)

$$PIGCD = \frac{B \cdot TOXE}{V_{gsteff}^{\ 2}} \left(1 - \frac{V_{dseff}}{2 \cdot V_{gsteff}} \right)$$