Chapter 8: High-Speed/RF Models

As circuit speed and operating frequency rise, the need for accurate prediction of circuit performance near cut-off frequency or under very rapid transient operation becomes critical. BSIM4.0.0 provides a set of accurate and efficient high-speed/RF (radio frequency) models which consist of three modules: charge-deficit non-quasi-static (NQS) model, intrinsic-input resistance (IIR) model (bias-dependent gate resistance model), and substrate resistance network model. The charge-deficit NQS model comes from BSIM3v3.2 NQS model [11] but many improvements are added in BSIM4. The IIR model considers the effect of channel-reflected gate resistance and therefore accounts for the first-order NQS effect [12]. Thus, the charge-deficit NQS model and the IIR model should not be turned on simultaneously. These two models both work with multi-finger configuration. The substrate resistance model does not include any geometry dependence.

8.1 Charge-Deficit Non-Quasi-Static (NQS) Model

BSIM4 uses two separate model selectors to turn on or off the charge-deficit NQS model in transient simulation (using ***trnqsMod***) and AC simulation (using ***acnqsMod***). The AC NQS model does not require the internal NQS charge node that is needed for the transient NQS model. The transient and AC NQS models are developed from the same fundamental physics: the channel/gate charge response to the external signal are relaxation-time (t) dependent and the transcapacitances

and transconductances (such as G_m) for AC analysis can therefore be expressed as functions of jwt.

MOSFET channel region is analogous to a bias-dependent RC distributed transmission line (Figure 8-1a). In the Quasi-Static (QS) approach, the gate capacitor node is lumped with the external source and drain nodes (Figure 8-1b). This ignores the finite time for the channel charge to build-up. One way to capture the NQS effect is to represent the channel with *n* transistors in series (Figure 8-1c), but it comes at the expense of simulation time. The BSIM4 charge-deficit NQS model uses Elmore equivalent circuit to model channel charge build-up, as illustrated in Figure 8-1d..

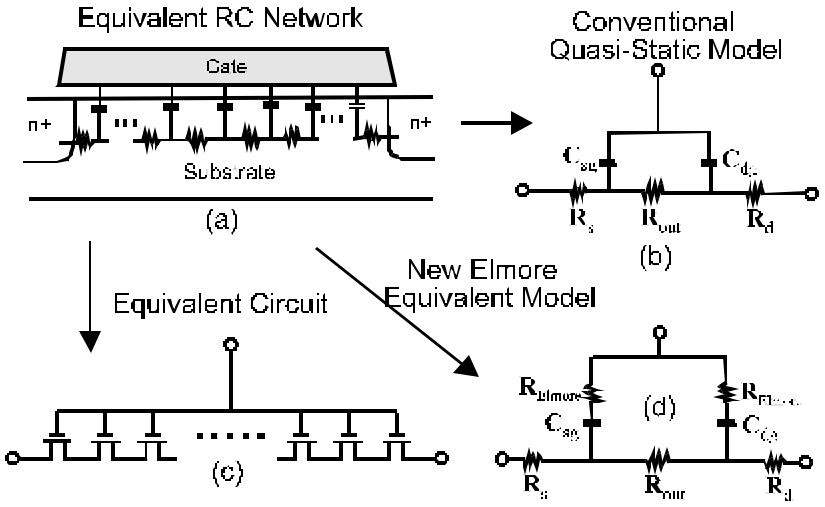


Figure 8-1. Quasi-Static and Non-Quasi-Static models for SPICE analysis.

8.1.1 The Transient Model

The transient charge-deficit NQS model can be turned on by setting ***trnqsMod*** = 1 and off by setting ***trnqsMod*** = 0.

Figure 8-2 shows the RC sub-circuit of charge deficit NQS model for transient simulation [13]. An internal node, $Q_{def}(t)$, is created to keep track of the amount of deficit/surplus channel charge necessary to reach equilibrium. The resistance ***R*** is determined from the RC time constant (t). The current source $i_{cheq}(t)$ represents the equilibrium channel charging effect. The capacitor ***C*** is to be the value of C_{fact} (with a typical value of 1×10^{-9} Farad [11]) to improve simulation accuracy. Q_{def} now becomes

$$Q_{def}(t) = V_{def} \times C_{fact} \tag{8.1.1}$$

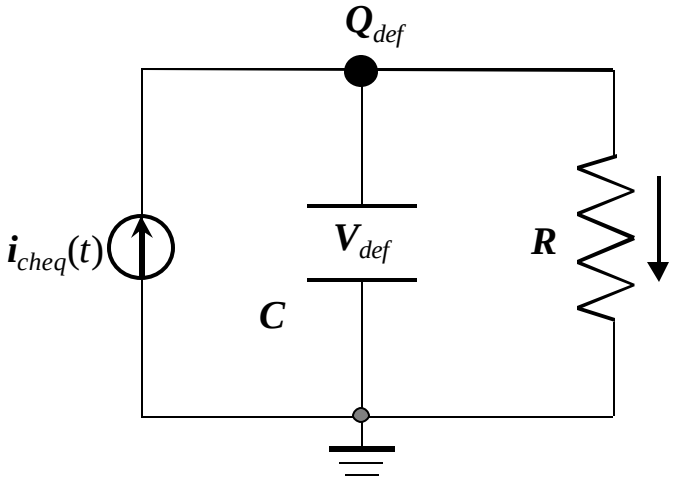


Figure 8-2. Charge deficit NQS sub-circuit for transient analysis.

Considering both the transport and charging component, the total current related to the terminals D, G and S can be written as

(8.1.2)

$$i_{D,G,S}(t) = I_{D,G,S}(\mathrm{DC}) + \frac{\partial Q_{d,g,s}(t)}{\partial t}$$

Based on the relaxation time approach, the terminal charge and corresponding charging current are modeled by

(8.1.3)

$$Q_{def}(t) = Q_{cheq}(t) - Q_{ch}(t)$$

and

(8.1.4a)

$$\frac{\partial Q_{def}(t)}{\partial t} = \frac{\partial Q_{cheq}(t)}{\partial t} - \frac{Q_{def}(t)}{t}$$

(8.1.4b)

$$\frac{\partial Q_{d,g,s}(t)}{\partial t} = D, G, S_{xpart}\,\frac{Q_{def}(t)}{t}$$

where D,G,S_{xpart} are charge deficit NQS channel charge partitioning number for terminals D, G and S, respectively; $D_{xpart} + S_{xpart} = 1$ and $G_{xpart} = -1$.

The transit time t is equal to the product of R_{ii} and $W_{eff}L_{eff}C_{oxe}$, where R_{ii} is the intrinsic-input resistance [12] given by

(8.1.5)

$$\frac{1}{R_{ii}} = XRCRG1 \cdot \left(\frac{I_{ds}}{V_{dseff}} + XRCRG2 \cdot \frac{W_{eff} m_{eff} C_{oxeff} k_B T}{q L_{eff}} \right)$$

where C_{oxeff} is the effective gate dielectric capacitance calculated from the DC model. Note that R_{ii} in (8.1.5) considers both the drift and diffusion componets of the channel conduction, each of which dominates in inversion and subthreshold regions, respectively.

8.1.2 The AC Model

Similarly, the small-signal AC charge-deficit NQS model can be turned on by setting ***acnqsMod*** = 1 and off by setting ***acnqsMod*** = 0.

For small signals, by substituting (8.1.3) into (8.1.4b), it is easy to show that in the frequency domain, $Q_{ch}(t)$ can be transformed into

(8.1.6)

$$\Delta Q_{ch}(t) = \frac{\Delta Q_{cheq}(t)}{1 + jwt}$$

where w is the angular frequency. Based on (8.1.6), it can be shown that the transcapacitances C_{gi}, C_{si}, and C_{di} (i stands for any of the G, D, S and B terminals of the device) and the channel transconductances G_m, G_{ds}, and G_{mbs} all become complex quantities. For example, now G_m have the form of

(8.1.7)

$$G_m = \frac{G_{m0}}{1+w^2t^2} + j\left(-\frac{G_{m0}\cdot wt}{1+w^2t^2}\right)$$

and

(8.1.8)

$$C_{dg} = \frac{C_{dg0}}{1+w^2t^2} + j\left(-\frac{C_{dg0}\cdot wt}{1+w^2t^2}\right)$$

Those quantities with sub "0" in the above two equations are known from OP (operating point) analysis.

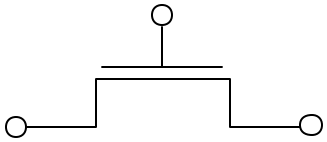
8.2 Gate Electrode Electrode and Intrinsic-Input Resistance (IIR) Model

8.2.1 General Description

BSIM4 provides four options for modeling gate electrode resistance (bias-independent) and intrinsic-input resistance (IIR, bias-dependent). The IIR model considers the relaxation-time effect due to the distributive RC nature of the channel region, and therefore describes the first-order non-quasi-static effect. Thus, the IIR model should not be used together with the charge-deficit NQS model at the same time. The model selector ***rgateMod*** is used to choose different options.

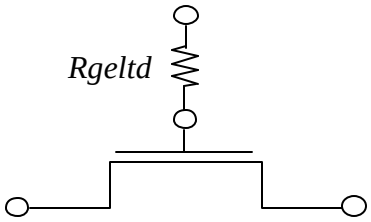
8.2.2 Model Option and Schematic

rgateMod = 0 (zero-resistance):



In this case, no gate resistance is generated.

rgateMod = 1 (constant-resistance):



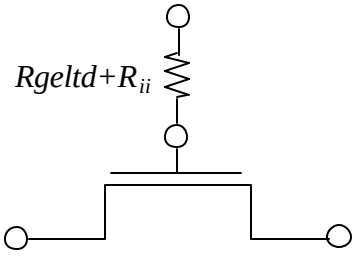
In this case, only the electode gate resistance (bias-independent) is generated by adding an internal gate node. Rgeltd is give by

(8.1.9)

$$Rgeltd = \frac{RSHG \cdot \left(XGW + \frac{W_{effcj}}{3 \cdot NGCON}\right)}{NGCON \cdot \left(L_{drawn} - XGL\right) \cdot NF}$$

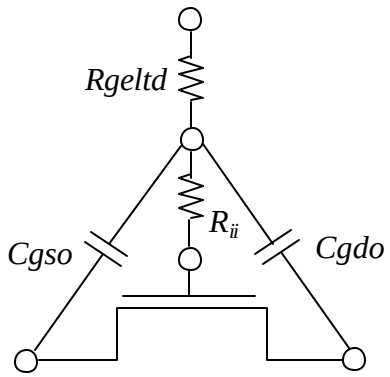
Refer to Chapter 7 for the layout parameters in the above equation.

rgateMod = 2 (IIR model with variable resistance):



In this case, the gate resistance is the sum of the electrode gate resistance (8.1.9) and the intrinsic-input resistance R_{ii} as given by (8.1.5). An internal gate node will be generated. ***trnqsMod*** = 0 (default) and ***acnqsMod*** = 0 (default) should be selected for this case.

rgateMod = 3 (IIR model with two nodes):



In this case, the gate electrode resistance given by (8.1.9) is in series with the intrinsic-input resistance R_{ii} as given by (8.1.5) through two internal gate nodes, so that the overlap capacitance current will not pass through the intrinsic-input resistance. ***trnqsMod*** = 0 (default) and ***acnqsMod*** = 0 (default) should be selected for this case.

8.3 Substrate Resistance Network

8.3.1 General Description

For CMOS RF circuit simulation, it is essential to consider the high frequency coupling through the substrate. BSIM4 offers a flexible built-in substrate resistance network. This network is constructed such that little simulation efficiency penalty will result. Note that the substrate resistance parameters as listed in Appendix A should be extracted for the total device, not on a per-finger basis.

8.3.2 Model Selector and Topology

The model selector ***rbodyMod*** can be used to turn on or turn off the resistance network.

rbodyMod = 0 (Off):

No substrate resistance network is generated at all.

rbodyMod = 1 (On):

All five resistances in the substrate network as shown schematically below are present simultaneously.

A minimum conductance, *GBMIN*, is introduced in parallel with each resistance and therefore to prevent infinite resistance values, which would otherwise cause poor convergence. In Figure 8-3, *GBMIN* is merged into each resistance to simplify the representation of the model topology. Note that the intrinsic model substrate reference point in this case is the internal body node **bNodePrime**, into which the impact ionization current I_{ii} and the GIDL current I_{GIDL} flow.

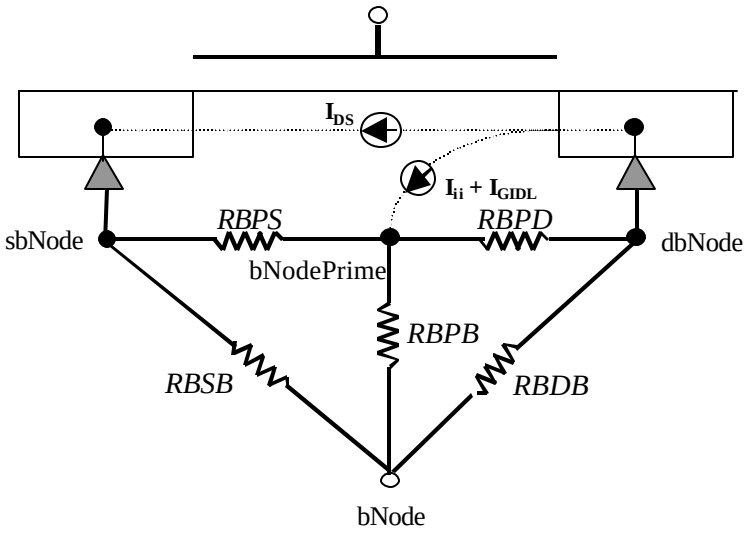


Figure 8-3. Topology with the substrate resistance network turned on.