BSIM4.2.1 MOSFET Model

- User's Manual

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Web Sites:

BSIM4 web site with BSIM source code and documents:

http://www-device.eecs.berkeley.edu/bsim3/~bsim4.html

Compact Model Council: **http://www.eigroup.org/~CMC**

Preface

BSIM4, as the extension of BSIM3 model, addresses the MOSFET physical effects into sub-100nm regime.

The continuous scaling of minimum feature size brought challenges to compact modeling in two ways: One is that to push the barriers in making transistors with shorter gate length, advanced process technologies are used such as non-uniform substrate doping. The second is its opportunities to RF applications.

To meet these challenges, BSIM4 has the following major improvements and additions over BSIM3v3:

(1) An accurate new model of the intrinsic input resistance for both RF, high-frequency analog and high-speed digital applications;

(2) An accurate gate direct tunneling model;

(3) A gate-induced drain/source leakage (GIDL/ GISL) current model, available in BSIM for the first time;

(4) Flexible substrate resistance network for RF modeling;

Other improvements include: 5) A new accurate channel thermal noise model and a noise partition model for the induced gate noise; 6)A non-quasi-static (NQS) model that is consistent with the Rg-based RF model and a consistent AC model that accounts for the NQS effect in both transconductances and capacitances. 7)A comprehensive and versatile geometry-dependent parasitics model for various source/drain connections and multi-finger devices; 8)Improved model for steep vertical retrograde doping profiles; 9)Better model for pocket-implanted devices in Vth, bulk charge effect model, and Rout; 10)Asymmetrical and bias-dependent source/ drain resistance, either internal or external to the intrinsic MOSFET at the user's discretion; 11)Acceptance of either the electrical or physical gate oxide thickness as the model input at the user's choice in a physically accurate manner; 12)The quantum mechanical charge-layer-thickness model for both IV and CV; 13) A more accurate mobility model for predictive modeling; 14)An improved unified flicker (1/f) noise model, which is smooth over all bias regions and considers the bulk charge effect; 15)Different diode IV and CV characteristics for source and drain junctions; 16)Junction diode breakdown with or without current limiting; 17)Dielectric constant of the gate dielectric as a model parameter.