Chapter 7: Capacitance Model

Accurate modeling of MOSFET capacitance plays equally important role as that of the DC model. This chapter describes the methodology and device physics considered in both intrinsic and extrinsic capacitance modeling in BSIM4.0.0. Complete model parameters can be found in Appendix A.

7.1 General Description

BSIM4.0.0 provides three options for selecting intrinsic and overlap/fringing capacitance models. These capacitance models come from BSIM3v3.2, and the BSIM3v3.2 capacitance model parameters are used without change in BSIM4. except that separate *CKAPPA* parameters are introduced for the source-side and drain-side overlap capacitances. The BSIM3v3.2 ***capMod*** = 1 is no longer supported in BSIM4. The following table maps the BSIM4 capacitance models to those of BSIM3v3.2.

BSIM4 capacitance models	Matched *capMod* in BSIM3v3.2.2
capMod = 0 (simple and piece-wise model)	Intrinsic ***capMod*** = 0 + overlap/fringing ***capMod*** = 0
capMod = 1 (single-equation model)	Intrinsic ***capMod*** = 2 + overlap/fringing ***capMod*** = 2
capMod = 2 (default model; singel-equation and charge-thickness model	Intrinsic ***capMod*** = 3 + overlap/fringing ***capMod*** = 2

Table 7-1. BSIM4 capacitance model options.

BSIM4 capacitance models have the following features:

- Separate effective channel length and width are used for capacitance models.
- ***capMod*** = 0 uses piece-wise equations. ***capMod*** = 1 and 2 are smooth and single equation models; therefore both charge and capacitance are continous and smooth over all regions.
- Threshold voltage is consistent with DC part except for ***capMod*** = 0, where a long-channel V_{th} is used. Therefore, those effects such as body bias, short/narrow channel and DIBL effects are explicitly considered in ***capMod*** = 1 and 2.
- Overlap capacitance comprises two parts: (1) a bias-independent component which models the effective overlap capacitance between the gate and the heavily doped source/drain; (2) a gate-bias dependent component between the gate and the lightly doped source/drain region.
- Bias-independent fringing capacitances are added between the gate and source as well as the gate and drain.

7.2 Methodology for Intrinsic Capacitance Modeling

7.2.1 Basic Formulation

To ensure charge conservation, terminal charges instead of terminal voltages are used as state variables. The terminal charges Q_g, Q_b, Q_s, and Q_d are the charges associated with the gate, bulk, source, and drain termianls, respectively. The gate charge is comprised of mirror charges from these components: the channel charge (Q_{inv}), accumulation charge (Q_{acc}) and substrate depletion charge (Q_{sub}).

The accumulation charge and the substrate charge are associated with the substrate while the channel charge comes from the source and drain terminals

$$\begin{cases} Q_g = -\left(Q_{sub} + Q_{inv} + Q_{acc}\right) \\ Q_b = Q_{acc} + Q_{sub} \\ Q_{inv} = Q_s + Q_d \end{cases} \tag{7.2.1}$$

The substrate charge can be divided into two components: the substrate charge at zero source-drain bias (Q_{sub0}), which is a function of gate to substrate bias, and the additional non-uniform substrate charge in the presence of a drain bias (dQ_{sub}). Q_g now becomes

$$Q_g = -\left(Q_{inv} + Q_{acc} + Q_{sub0} + dQ_{sub}\right) \tag{7.2.2}$$

The total charge is computed by integrating the charge along the channel. The threshold voltage along the channel is modified due to the non-uniform substrate charge by

(7.2.3)

$$V_{th}(y) = V_{th}(0) + (A_{bulk} - 1)V_y$$

(7.2.4)

$$\begin{cases} Q_c = W_{active}\int_0^{L_{active}} q_c dy = -W_{active}C_{oxe}\int_0^{L_{active}}\left(V_{gt} - A_{bulk}V_y\right)dy \\ Q_g = W_{active}\int_0^{L_{active}} q_g dy = W_{active}C_{oxe}\int_0^{L_{active}}\left(V_{gt} + V_{th} - V_{FB} - \Phi_s - V_y\right)dy \\ Q_b = W_{active}\int_0^{L_{active}} q_b dy = -W_{active}C_{oxe}\int_0^{L_{active}}\left(V_{th} - V_{FB} - \Phi_s + \left(A_{bulk} - 1\right)V_y\right)dy \end{cases}$$

where $V_{gt} = V_{gse} - V_{th}$ and

$$dy = \frac{dV_y}{E_y}$$

where E_y is expressed in

(7.2.5)

$$I_{ds} = \frac{W_{active}m_{eff}C_{oxe}}{L_{active}}\left(V_{gt} - \frac{A_{bulk}}{2}V_{ds}\right)V_{ds} = W_{active}m_{eff}C_{oxe}\left(V_{gt} - A_{bulk}V_y\right)E_y$$

All capacitances are derived from the charges to ensure charge conservation. Since there are four terminals, there are altogether 16 components. For each component

(7.2.6)

$$C_{ij} = \frac{\partial Q_i}{\partial V_j}$$

where *i* and *j* denote the transistor terminals. C_{ij} satisfies

$$\sum_i C_{ij} = \sum_j C_{ij} = 0$$

7.2.2 Short Channel Model

The long-channel charge model assume a constant mobility with no velocity saturation. Since no channel length modulation is considered, the channel charge remains constant in saturation region. Conventional long-channel charge models assume $V_{dsat,CV} = V_{gt} / A_{bulk}$ and therefore is independent of channel length. If we define a drain bias, $V_{dsat,CV}$, for capacitance modeling, at which the channel charge becomes constant, we will find that $V_{dsat,CV}$ in general is larger than V_{dsat} for I-V but smaller than the long-channel $V_{dsat} = V_{gt} / A_{bulk}$. In other words,

(7.2.7)

$$V_{dsat,IV} < V_{dsat,CV} < V_{dsat,IV}\Big|_{Lactive \to \infty} = \frac{V_{gsteff,CV}}{A_{bulk}}$$

and $V_{dsat,CV}$ is modeled by

(7.2.8)

$$V_{dsat,CV} = \frac{V_{gsteff,CV}}{A_{bulk} \cdot \left[1 + \left(\frac{CLC}{L_{active}}\right)^{CLE}\right]}$$

(7.2.9)

$$V_{gsteff,CV} = NOFF \cdot nv_t \cdot \ln\left[1+\exp\left(\frac{V_{gse}-V_{th}-VOFFCV}{NOFF \cdot nv_t}\right)\right]$$

Model parameters *CLC* and *CLE* are introduced to consider the effect of channel-length modulation. A_{bulk} for the capacitance model is modeled by

(7.2.10)

$$A_{bulk} = \left\{1+ F\_doping \cdot \left[\frac{A0 \cdot L_{eff}}{L_{eff}+2\sqrt{XJ \cdot X_{dep}}} \cdot + \frac{B0}{W_{eff}'+B1}\right] \cdot \right\} \frac{1}{1+ KETA \cdot V_{bseff}}$$

where

$$F\_doping = \frac{\sqrt{1+LPEB/L_{eff}}K_{1ox}}{2\sqrt{\Phi_s - V_{bseff}}} + K_{2ox} - K3B\frac{TOXE}{W_{eff}'+W0}\Phi_s$$

7.2.3 Single Equation Formulation

Traditional MOSFET SPICE capacitance models use piece-wise equations. This can result in discontinuities and non-smoothness at transition regions. The following describes single-equation formulation for charge, capacitance and voltage modeling in ***capMod*** = 1 and 2.

(a) Transition from depletion to inversion region

The biggest discontinuity is at threshold voltage where the inversion capacitance changes abruptly from zero to C_{oxe}. Concurrently, since the substrate charge is a constant, the substrate capacitance drops abruptly to

zero at threshold voltage. The BSIM4 charge and capacitance models are formulated by substituting V_{gst} with $V_{gsteff,CV}$ as

(7.2.11)

$$Q(V_{gst}) = Q(V_{gsteff,CV})$$

For capacitance modeling

(7.2.12)

$$C(V_{gst}) = C(V_{gsteff,CV})\frac{\partial V_{gsteff,CV}}{V_{g,d,s,b}}$$

(b) Transition from accumulation to depletion region

An effective smooth flatband voltage V_{FBeff} is used for the accumulation and depletion regions.

(7.2.13)

$$V_{FBeff} = V_{fbzb} - 0.5\left[(V_{fbzb} - V_{gb} - 0.02) + \sqrt{(V_{fbzb} - V_{gb} - 0.02)^2 + 0.08V_{fbzb}}\right]$$

where

(7.2.14)

$$V_{fbzb} = V_{th}\Big|_{zero V_{bs} and V_{ds}} - \Phi_s - K1\sqrt{\Phi_s}$$

A bias-independent V_{th} is used to calculate V_{fbzb} for ***capMod*** = 1 and 2. For ***capMod*** = 0, *VFBCV* is used instead (refer to Appendix A).

(c) Transition from linear to saturation region

An effective V_{ds}, V_{cveff}, is used to smooth out the transition between linear and saturation regions.

(7.2.15)

$$V_{cveff} = V_{dsat,CV} - 0.5\left\{V_4 + \sqrt{V_4^2 + 4d_4 V_{dsat,CV}}\right\} \quad where V_4 = V_{dsat,CV} - V_{ds} - d_4;\ d_4 = 0.02V$$

7.2.4 Charge partitioning

The inversion charges are partitioned into $Q_{inv} = Q_s + Q_d$. The ratio of Q_d to Q_s is the charge partitioning ratio. Existing charge partitioning schemes are 0/100, 50/50 and 40/60 (*XPART* = 1, 0.5 and 0).

50/50 charge partition

This is the simplest of all partitioning schemes in which the inversion charges are assumed to be contributed equally from the source and drain terminals.

40/60 charge partition

This is the most physical model of the three partitioning schemes in which the channel charges are allocated to the source and drain terminals by assuming a linear dependence on channel position *y*.

(7.2.16)

$$\begin{cases} Q_s = W_{active} \int_0^{L_{active}} q_c \left(1 - \frac{y}{L_{active}}\right) dy \\ Q_d = W_{active} \int_0^{L_{active}} q_c \frac{y}{L_{active}} dy \end{cases}$$

0/100 charge partition

In fast transient simulations, the use of a quasi-static model may result in a large unrealistic drain current spike. This partitioning scheme is developed to artificially suppress the drain current spike by assigning all inversion charges in the saturation region to the source electrode. Notice that this charge partitioning scheme will still give drain current spikes in the linear region and aggravate the source current spike problem.

7.3 Charge-Thickness Capacitance Model (CTM)

Current MOSFET models in SPICE generally overestimate the intrinsic capacitance and usually are not smooth at V_{fb} and V_{th}. The discrepancy is more pronounced in thinner T_{ox} devices due to the assumption of inversion and accumulation charge being located at the interface. Numerical quantum simulation results in Figure 7-1 indicate the significant charge thickness in all regions of operation.

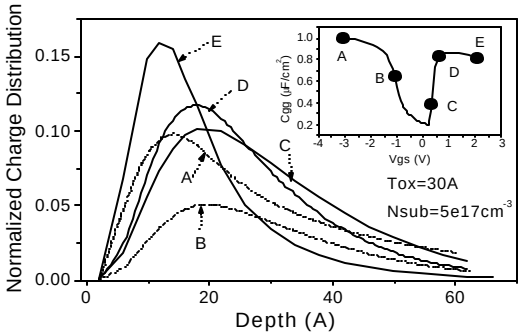

Figure 7-1. Charge distribution from numerical quantum simulations show significant charge thickness at various bias conditions shown in the inset.

CTM is a charge-based model and therefore starts with the DC charge thicknss, X_{DC}. The charge thicknss introduces a capacitance in series with C_{ox} as illustrated in Figure 7-2, resulting in an effective C_{oxeff}. Based on numerical self-consistent solution of Shrodinger, Poisson and Fermi-Dirac equations, universal and analytical X_{DC} models have been developed. C_{oxeff} can be expressed as

(7.3.1)

$$C_{oxeff} = \frac{C_{oxe} \cdot C_{cen}}{C_{oxe} + C_{cen}}$$

where

$$C_{cen} = \varepsilon_{si} / X_{DC}$$

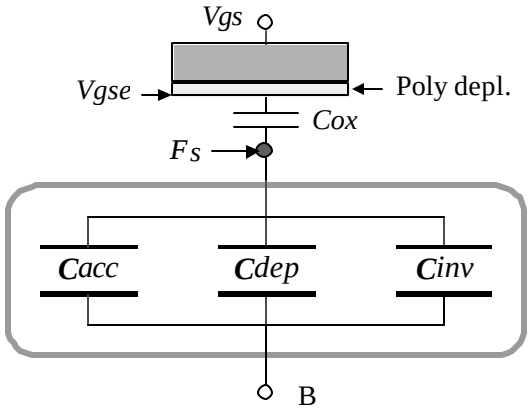

Figure 7-2. Charge-thickness capacitance concept in CTM. V_{gse} accounts for the poly depletion effect.

(i) X_{DC} for accumulation and depletion

The DC charge thickness in the accumulation and depletion regions can be expressed by

(7.3.2)

$$X_{DC} = \frac{1}{3} L_{debye} \exp\left[ACDE \cdot \left(\frac{NDEP}{2\times 10^{16}} \right)^{-0.25} \cdot \frac{V_{gse} - V_{bseff} - V_{FBeff}}{TOXE} \right]$$

where L_{debye} is Debye length, and X_{DC} is in the unit of cm and (V_{gse} - V_{bseff} - V_{FBeff}) / *TOXE* is in units of MV/cm. For numerical statbility, (7.3.2) is replaced by (7.3.3)

(7.3.3)

$$X_{DC} = X_{\max} - \frac{1}{2}\left(X_0 + \sqrt{X_0^2 + 4d_x X_{\max}} \right)$$

where

$$X_0 = X_{\max} - X_{DC} - d_x$$

and $X_{max} = L_{debye} / 3$; $\delta_x = 10^{-3} TOXE$.

(ii) X_{DC} of inversion charge

The inversion charge layer thichness can be formulated as

(7.3.4)

$$X_{DC} = \frac{1.9\times10^{-9}\ \text{cm}}{1+\left(\frac{V_{gsteff}+4(VTH0-VFB-\Phi_s)}{2TOXP}\right)^{0.7}}$$

Through the *VFB* term, equation (7.3.4) is found to be applicable to N^+ or P^+ poly-Si gates and even other future gate materials.

(iii) Body charge thichness in inversion

In inversion region, the body charge thickness effect is modeled by including the deviation of the surface potential Φ_s (bias-dependence) from $2\Phi_B$ [2]

(7.3.5)

$$j_d = \Phi_s - 2\Phi_B = n_t \ln\left(\frac{V_{gsteffCV}\cdot(V_{gsteffCV}+2K_{1ox}\sqrt{2\Phi_B}}{MOIN\cdot K_{1ox}{}^2 n_t}\right)$$

The channel charge density is therefore derived as

(7.3.6)

$$q_{inv} = -C_{oxeff}\cdot\left(V_{gsteff,CV} - j_d\right)$$

7.4 Intrinsic Capacitance Model Equations

7.4.1 *capMod* = 0

Accumulation region

$$Q_g = W_{active} L_{active} C_{oxe} \left(V_{gs} - V_{bs} - VFBCV \right)$$

$$Q_{sub} = -Q_g$$

$$Q_{inv} = 0$$

Subthreshold region

$$Q_{sub0} = -W_{active} L_{active} C_{oxe} \cdot \frac{K_{1ox}{}^2}{2} \left(-1 + \sqrt{1 + \frac{4\left(V_{gs} - VFBCV - V_{bs}\right)}{K_{1ox}{}^2}} \right)$$

$$Q_g = -Q_{sub0}$$

$$Q_{inv} = 0$$

Strong inversion region

$$V_{dsat,cv} = \frac{V_{gs} - V_{th}}{A_{bulk}{}'}$$

$$A_{bulk}{}' = A_{bulk} \left(1 + \left(\frac{CLC}{L_{eff}} \right)^{CLE} \right)$$

$$V_{th} = VFBCV + \Phi_s + K_{1ox} \sqrt{\Phi_s - V_{bseff}}$$

Linear region

$$Q_g = C_{oxe} W_{active} L_{active} \left(V_{gs} - VFBCV - \Phi_s - \frac{V_{ds}}{2} + \frac{A_{bulk}' V_{ds}^{\ 2}}{12\left(V_{gs} - V_{th} - \frac{A_{bulk}' V_{ds}}{2} \right)} \right)$$

$$Q_b = C_{oxe} W_{active} L_{active} \left(VFBCV - V_{th} - \Phi_s + \frac{(1 - A_{bulk}') V_{ds}}{2} - \frac{(1 - A_{bulk}') A_{bulk}' V_{ds}^{\ 2}}{12\left(V_{gs} - V_{th} - \frac{A_{bulk}' V_{ds}}{2} \right)} \right)$$

50/50 partitioning:

$$Q_{inv} = -C_{oxe} W_{active} L_{active} \left(V_{gs} - V_{th} - \Phi_s - \frac{A_{bulk}' V_{ds}}{2} + \frac{A_{bulk}'^2 V_{ds}^{\ 2}}{12\left(V_{gs} - V_{th} - \frac{A_{bulk}' V_{ds}}{2} \right)} \right)$$

$$Q_s = Q_d = 0.5 Q_{inv}$$

40/60 partitioning:

$$Q_d = -C_{oxe} W_{active} L_{active} \left(\frac{V_{gs} - V_{th}}{2} - \frac{A_{bulk}' V_{ds}}{2} + \frac{A_{bulk}' V_{ds} \left[\frac{(V_{gs} - V_{th})^2}{6} - \frac{A_{bulk}' V_{ds} (V_{gs} - V_{th})}{8} + \frac{(A_{bulk}' V_{ds})^2}{40} \right]}{12\left(V_{gs} - V_{th} - \frac{A_{bulk}' V_{ds}}{2} \right)^2} \right)$$

$$Q_s = -(Q_g + Q_b + Q_d)$$

0/100 partitioning:

$$Q_d = -C_{oxe} W_{active} L_{active} \left(\frac{V_{gs} - V_{th}}{2} + \frac{A_{bulk}' V_{ds}}{4} - \frac{(A_{bulk}' V_{ds})^2}{24} \right)$$

$$Q_s = -(Q_g + Q_b + Q_d)$$

Saturation region

$$Q_g = C_{oxe} W_{active} L_{active} \left(V_{gs} - VFBCV - \Phi_s - \frac{V_{dsat}}{3} \right)$$

$$Q_b = -C_{oxe} W_{active} L_{active} \left(VFBCV + \Phi_s - V_{th} + \frac{(1 - A_{bulk}')V_{dsat}}{3} \right)$$

50/50 partitioning:

$$Q_s = Q_d = -\frac{1}{3} C_{oxe} W_{active} L_{active} (V_{gs} - V_{th})$$

40/60 partitioning:

$$Q_d = -\frac{4}{15} C_{oxe} W_{active} L_{active} (V_{gs} - V_{th})$$

$$Q_s = -(Q_g + Q_b + Q_d)$$

0/100 partitioning:

$$Q_d = 0$$

$$Q_s = -(Q_g + Q_b)$$

7.4.2 *capMod* = 1

$$Q_g = -(Q_{inv} + Q_{acc} + Q_{sub0} + dQ_{sub})$$

$$Q_b = -(Q_{acc} + Q_{sub0} + dQ_{sub})$$

$$Q_{inv} = Q_s + Q_d$$

$$Q_{acc} = -W_{active}L_{active}C_{oxe}\cdot\left(V_{FBeff} - V_{fbzb}\right)$$

$$Q_{sub0} = -W_{active}L_{active}C_{oxe}\cdot\frac{K_{1ox}{}^{2}}{2}\cdot\left[-1+\sqrt{1+\frac{4\left(V_{gse} - V_{FBeff} - V_{gsteff} - V_{bseff}\right)}{K_{1ox}{}^{2}}}\right]$$

$$V_{dsat,cv} = \frac{V_{gsteffcv}}{A_{bulk}{}'}$$

$$Q_{inv} = -W_{active}L_{active}C_{oxe}\cdot\left[V_{gsteff,cv} - \frac{1}{2}A_{bulk}{}'V_{cveff} + \frac{A_{bulk}{}'^{2}V_{cveff}^{2}}{12\cdot\left(V_{gsteff,cv} - A_{bulk}{}'V_{cveff}/2\right)}\right]$$

$$dQ_{sub} = W_{active}L_{active}C_{oxe}\cdot\left[\frac{1-A_{bulk}{}'}{2}V_{cveff} - \frac{\left(1-A_{bulk}{}'\right)\cdot A_{bulk}{}'V_{cveff}^{2}}{12\cdot\left(V_{gsteff,cv} - A_{bulk}{}'V_{cveff}/2\right)}\right]$$

50/50 charge partitioning:

$$Q_S = Q_D = -\frac{W_{active}L_{active}C_{oxe}}{2}\left[V_{gsteff,cv} - \frac{1}{2}A_{bulk}{}'V_{cveff} + \frac{A_{bulk}{}'^{2}V_{cveff}^{2}}{12\cdot\left(V_{gsteff,cv} - A_{bulk}{}'V_{cveff}/2\right)}\right]$$

40/60 charge partitioning:

$$Q_S = -\frac{W_{active}L_{active}C_{oxe}}{2\left(V_{gsteff,cv} - A_{bulk}'V_{cveff}/2\right)^2}\left[\begin{array}{l} V_{gsteff,cv}{}^3 - \frac{4}{3}V_{gsteff,cv}{}^2 A_{bulk}'V_{cveff} \\ + \frac{2}{3}V_{gsteff,cv}\left(A_{bulk}'V_{cveff}\right)^2 - \frac{2}{15}\left(A_{bulk}'V_{cveff}\right)^3 \end{array}\right]$$

$$Q_D = -\frac{W_{active}L_{active}C_{oxe}}{2\left(V_{gsteff,cv} - A_{bulk}'V_{cveff}/2\right)^2}\left[\begin{array}{l} V_{gsteff,cv}{}^3 - \frac{5}{3}V_{gsteff,cv}{}^2 A_{bulk}'V_{cveff} \\ + V_{gsteff,cv}\left(A_{bulk}'V_{cveff}\right)^2 - \frac{1}{5}\left(A_{bulk}'V_{cveff}\right)^3 \end{array}\right]$$

0/100 charge partitioning:

$$Q_S = -\frac{W_{active}L_{active}C_{oxe}}{2}\cdot\left[V_{gsteff,cv} + \frac{1}{2}A_{bulk}'V_{cveff} - \frac{A_{bulk}'^2 V_{cveff}^2}{12\cdot\left(V_{gsteff,cv} - A_{bulk}'V_{cveff}/2\right)}\right]$$

$$Q_D = -\frac{W_{active}L_{active}C_{oxe}}{2}\cdot\left[V_{gsteff,cv} - \frac{3}{2}A_{bulk}'V_{cveff} + \frac{A_{bulk}'^2 V_{cveff}^2}{4\cdot\left(V_{gsteff,cv} - A_{bulk}'V_{dveff}/2\right)}\right]$$

7.4.3 *capMod* = 2

$$Q_{acc} = W_{active}L_{active}C_{oxeff}\cdot V_{gbacc}$$

$$V_{gbacc} = \frac{1}{2}\cdot\left[V_0 + \sqrt{V_0^2 + 0.08V_{fbzb}}\right]$$

$$V_0 = V_{fbzb} + V_{bseff} - V_{gs} - 0.02$$

$$V_{cveff} = V_{dsat} - \frac{1}{2}\cdot\left(V_1 + \sqrt{V_1^{\,2} + 0.08V_{dsat}}\right)$$

$$V_1 = V_{dsat} - V_{ds} - 0.02$$

$$V_{dsat} = \frac{V_{gsteff,cv} - j_d}{A_{bulk}'}$$

$$j_d = \Phi_s - 2\Phi_B = n_t \ln\left(\frac{V_{gsteffCV}\cdot(V_{gsteffCV} + 2K_{1ox}\sqrt{2\Phi_B}}{MOIN\cdot K_{1ox}^{\,2} n_t}\right)$$

$$Q_{sub0} = -W_{active}L_{active}C_{oxeff}\cdot\frac{K_{1ox}^{\,2}}{2}\cdot\left[-1+\sqrt{1+\frac{4\left(V_{gse}-V_{FBeff}-V_{bseffs}-V_{gsteff,cv}\right)}{K_{1ox}^{\,2}}}\right]$$

$$Q_{inv} = -W_{active}L_{active}C_{oxeff}\cdot\left[V_{gsteff,cv} - j_d - \frac{1}{2}A_{bulk}'V_{cveff} + \frac{A_{bulk}'^{2}V_{cveff}^{2}}{12\cdot\left(V_{gsteff,cv} - j_d - A_{bulk}'V_{cveff}/2\right)}\right]$$

$$dQ_{sub} = W_{active}L_{active}C_{oxeff}\cdot\left[\frac{1-A_{bulk}'}{2}V_{cveff} - \frac{\left(1-A_{bulk}'\right)\cdot A_{bulk}'V_{cveff}^{2}}{12\cdot\left(V_{gsteff,cv} - j_d - A_{bulk}'V_{cveff}/2\right)}\right]$$

50/50 partitioning:

$$Q_S = Q_D = -\frac{W_{active}L_{active}C_{oxeff}}{2}\left[V_{gsteff,cv} - j_d - \frac{1}{2}A_{bulk}'V_{cveff} + \frac{A_{bulk}'^{2}V_{cveff}^{2}}{12\cdot\left(V_{gsteff,cv} - j_d - A_{bulk}'V_{cveff}/2\right)}\right]$$

40/60 partitioning:

$$Q_S = -\frac{W_{active}L_{active}C_{oxeff}}{2\left(V_{gsteff,cv} - j_d - A_{bulk}'V_{cveff}/2\right)^2}\left[\begin{array}{l}\left(V_{gsteff,cv} - j_d\right)^3 - \frac{4}{3}\left(V_{gsteff,cv} - j_d\right)^2 A_{bulk}'V_{cveff} \\ + \frac{2}{3}\left(V_{gsteff,cv} - j_d\right)\left(A_{bulk}'V_{cveff}\right)^2 - \frac{2}{15}\left(A_{bulk}'V_{cveff}\right)^3\end{array}\right]$$

$$Q_D = -\frac{W_{active}L_{active}C_{oxeff}}{2\left(V_{gsteff,cv} - j_d - A_{bulk}'V_{cveff}/2\right)^2}\left[\begin{array}{l}\left(V_{gsteff,cv} - j_d\right)^3 - \frac{5}{3}\left(V_{gsteff,cv} - j_d\right)^2 A_{bulk}'V_{cveff} \\ + \left(V_{gsteff,cv} - j_d\right)\left(A_{bulk}'V_{cveff}\right)^2 - \frac{1}{5}\left(A_{bulk}'V_{cveff}\right)^3\end{array}\right]$$

0/100 partitioning:

$$Q_S = -\frac{W_{active}L_{active}C_{oxeff}}{2}\cdot\left[V_{gsteff,cv} - j_d + \frac{1}{2}A_{bulk}'V_{cveff} - \frac{A_{bulk}'^2V_{cveff}^2}{12\cdot\left(V_{gsteff,cv} - j_d - A_{bulk}'V_{cveff}/2\right)}\right]$$

$$Q_D = -\frac{W_{active}L_{active}C_{oxeff}}{2}\cdot\left[V_{gsteff,cv} - j_d - \frac{3}{2}A_{bulk}'V_{cveff} + \frac{A_{bulk}'^2V_{cveff}^2}{4\cdot\left(V_{gsteff,cv} - j_d - A_{bulk}'V_{dveff}/2\right)}\right]$$

7.5 Fringing/Overlap Capacitance Models

7.5.1 Fringing capacitance model

The fringing capacitance consists of a bias-independent outer fringing capacitance and a bias-dependent inner fringing capacitance. Only the bias-independent outer fringing capacitance (*CF*) is modeled. If *CF* is not given, it is calculated by

(7.5.1)

$$CF = \frac{2 \cdot EPSROX \cdot \varepsilon_0}{\pi} \cdot \log\left(1 + \frac{4.0e-7}{TOXE}\right)$$

7.5.2 Overlap capacitance model

An accurate overlap capacitance model is essential. This is especially true for the drain side where the effect of the capacitance is amplified by the transistor gain. In old capacitance models this capacitance is assumed to be bias independent. However, experimental data show that the overlap capacitance changes with gate to source and gate to drain biases. In a single drain structure or the heavily doped S/D to gate overlap region in a LDD structure the bias dependence is the result of depleting the surface of the source and drain regions. Since the modulation is expected to be very small, we can model this region with a constant capacitance. However in LDD MOSFETs a substantial portion of the LDD region can be depleted, both in the vertical and lateral directions. This can lead to a large reduction of the overlap capacitance. This LDD region can be in accumulation or depletion. We use a single equation for both regions by using such smoothing parameters as $V_{gs,overlap}$ and $V_{gd,overlap}$ for the source and drain side, respectively. Unlike the case with the intrinsic capacitance, the overlap capacitances are reciprocal. In other words, $C_{gs,overlap} = C_{sg,overlap}$ and $C_{gd,overlap} = C_{dg,overlap}$.

If capMod is non-zero, BSIM4 uses the bias-dependent overlap capacitance model; otherwise, a simple bias-independent model will be used.

Bias-dependent overlap capacitance model

(i) Source side

(7.5.2)

$$\frac{Q_{overlaps}}{W_{active}} = CGSO \cdot V_{gs} + CGSL\left(V_{gs} - V_{gs,overlap} - \frac{CKAPPAS}{2}\left(-1 + \sqrt{1 - \frac{4V_{gs,overlap}}{CKAPPAS}} \right) \right)$$

(7.5.3)

$$V_{gs,overlap} = \frac{1}{2}\left(V_{gs} + d_1 - \sqrt{\left(V_{gs} + d_1\right)^2 + 4d_1} \right), \quad d_1 = 0.02V$$

(ii) Drain side

(7.5.4)

$$\frac{Q_{overlapd}}{W_{active}} = CGDO \cdot V_{gd} + CGDL\left(V_{gd} - V_{gd,overlap} - \frac{CKAPPAD}{2}\left(-1 + \sqrt{1 - \frac{4V_{gd,overlap}}{CKAPPAD}} \right) \right)$$

(7.5.5)

$$V_{gd,overlap} = \frac{1}{2}\left(V_{gd} + d_1 - \sqrt{\left(V_{gd} + d_1\right)^2 + 4d_1} \right), \quad d_1 = 0.02V$$

(iii) Gate Overlap Charge

(7.5.6)

$$Q_{overlap,g} = -\left(Q_{overlap,d} + Q_{overlap,s} + \left(CGBO \cdot L_{active}\right) \cdot V_{gb}\right)$$

where *CGBO* is a model parameter, which represents the gate-to-body overlap capacitance per unit channel length.

Bias-independent overlap capacitance model

If ***capMod*** = 0, a bias-independent overlap capacitance model will be used. In this case, model parameters *CGSL*, *CGDL*, *CKAPPAS* and *CKAPPD* all have no effect.

The gate-to-source overlap charge is expressed by

$$Q_{overlap,s} = W_{active} \cdot CGSO \cdot V_{gs}$$

The gate-to-drain overlap charge is calculated by

$$Q_{overlap,d} = W_{active} \cdot CGDO \cdot V_{gd}$$

The gate-to-substrate overlap charge is computed by

$$Q_{overlap,b} = L_{active} \cdot CGBO \cdot V_{gb}$$

Default *CGSO* and *CGDO*

If *CGSO* and *CGDO* (the overlap capacitances between the gate and the heavily doped source/drain regions, respectively) are not given, they will be calculated. Appendix A gives the information on how *CGSO*, *CGDO* and *CGBO* are calculated.