Chapter 10: Asymmetric MOS Junction Diode Models

10.1 Junction Diode IV Model

In BSIM4, there are three junction diode IV models. When the IV model selector ***dioMod*** is set to 0 ("resistance-free"), the diode IV is modeled as resistance-free with or without breakdown depending on the parameter values of *XJBVS* or *XJBVD*. When ***dioMod*** is set to 1 ("breakdown-free"), the diode is modeled exactly the same way as in BSIM3v3.2 with current-limiting feature in the forward-bias region through the limiting current parameters *IJTHSFWD* or *IJTHDFWD*; diode breakdown is not modeled for ***dioMod*** = 1 and *XJBVS*, *XJBVD*, *BVS*, and *BVD* parameters all have no effect. When ***dioMod*** is set to 2 ("resistance-and-breakdown"), BSIM4 models the diode breakdown with current limiting in both forward and reverse operations. In general, setting ***dioMod*** to 1 produces fast convergence.

10.1.1 Source/Body Junction Diode

In the following, the equations for the source-side diode are given. The model parameters are shown in Appendix A.

- ***dioMod* = 0 (resistance-free)**

(10.1.1)

$$I_{bs} = I_{sbs}\left[\exp\left(\frac{qV_{bs}}{NJS \cdot k_B TNOM}\right) - 1\right] \cdot f_{breakdown} + V_{bs} \cdot G_{\min}$$

where I_{sbs} is the total saturation current consisting of the components through the gate-edge (J_{sswgs}) and isolation-edge sidewalls (J_{ssws}) and the bottom junction (J_{ss}),

(10.1.2)

$$I_{sbs} = A_{seff} J_{ss}(T) + P_{seff} J_{ssws}(T) + W_{effcj} \cdot NF \cdot J_{sswgs}(T)$$

where the calculation of the junction area and perimeter is discussed in Chapter 11, and the temperature-dependent current density model is given in Chapter 12. In (10.1.1), $f_{breakdown}$ is given by

(10.1.3)

$$f_{breakdown} = 1 + XJBVS \cdot \exp\left(-\frac{q \cdot (BVS + V_{bs})}{NJS \cdot k_B TNOM}\right)$$

In the above equation, when *XJBVS* = 0, no breakdown will be modeled. If *XJBVS* < 0.0, it is reset to 1.0.

- ***dioMod* = 1 (breakdown-free)**

No breakdown is modeled. The exponential IV term in (10.1.4) is linearized at the limiting current *IJTHSFWD* in the forward-bias model only.

(10.1.4)

$$I_{bs} = I_{sbs}\left[\exp\left(\frac{qV_{bs}}{NJS \cdot k_B TNOM}\right) - 1\right] + V_{bs} \cdot G_{\min}$$

- ***dioMod* = 2 (resistance-and-breakdown):**

Diode breakdown is always modeled. The exponential term (10.1.5) is linearized at both the limiting current *IJTHSFWD* in the forward-bias mode and the limiting current *IJTHSREV* in the reverse-bias mode.

(10.1.5)

$$I_{bs} = I_{sbs}\left[\exp\left(\frac{qV_{bs}}{NJS \cdot k_B TNOM}\right) - 1\right] \cdot f_{breakdown} + V_{bs} \cdot G_{\min}$$

For ***dioMod*** = 2, if *XJBVS* <= 0.0, it is reset to 1.0.

6.1.2 Drain/Body Junction Diode

The drain-side diode has the same system of equations as those for the source-side diode, but with a separate set of model parameters as explained in detail in Appendix A.

- ***dioMod* = 0 (resistance-free)**

(10.1.6)

$$I_{bd} = I_{sbd}\left[\exp\left(\frac{qV_{bd}}{NJD \cdot k_B TNOM}\right) - 1\right] \cdot f_{breakdown} + V_{bd} \cdot G_{\min}$$

where I_{sbd} is the total saturation current consisting of the components through the gate-edge (J_{sswgd}) and isolation-edge sidewalls (J_{sswd}) and the bottom junction (J_{sd}),

(10.1.7)

$$I_{sbd} = A_{deff} J_{sd}(T) + P_{deff} J_{sswd}(T) + W_{effcj} \cdot NF \cdot J_{sswgd}(T)$$

where the calculation of the junction area and perimeter is discussed in Chapter 11, and the temperature-dependent current density model is given in Chapter 12. In (10.1.6), $f_{breakdown}$ is given by

(10.1.8)

$$f_{breakdown} = 1 + XJBVD \cdot \exp\left(-\frac{q \cdot (BVD + V_{bd})}{NJD \cdot k_B TNOM} \right)$$

In the above equation, when *XJBVD* = 0, no breakdown will be modeled. If *XJBVD* < 0.0, it is reset to 1.0.

- ***dioMod* = 1 (breakdown-free)**

No breakdown is modeled. The exponential IV term in (10.1.9) is linearized at the limiting current *IJTHSFWD* in the forward-bias model only.

(10.1.9)

$$I_{bd} = I_{sbd} \left[\exp\left(\frac{qV_{bd}}{NJD \cdot k_B TNOM} \right) - 1 \right] + V_{bd} \cdot G_{\min}$$

- ***dioMod* = 2 (resistance-and-breakdown):**

Diode breakdown is always modeled. The exponential term (10.1.10) is linearized at both the limiting current *IJTHSFWD* in the forward-bias mode and the limiting current *IJTHSREV* in the reverse-bias mode.

(10.1.10)

$$I_{bd} = I_{sbd}\left[\exp\left(\frac{qV_{bd}}{NJD \cdot k_B TNOM}\right) - 1\right] \cdot f_{breakdown} + V_{bd} \cdot G_{\min}$$

For ***dioMod*** = 2, if *XJBVD* <= 0.0, it is reset to 1.0.

10.2 Junction Diode CV Model

Source and drain junction capacitances consist of three components: the bottom junction capacitance, sidewall junction capacitance along the isolation edge, and sidewall junction capacitance along the gate edge. An analogous set of equations are used for both sides but each side has a separate set of model parameters.

10.2.1 Source/Body Junction Diode

The source-side junction capacitance can be calculated by

$$C_{bs} = A_{seff} C_{jbs} + P_{seff} C_{jbssw} + W_{effcj} \cdot NF \cdot C_{jbsswg} \tag{10.2.1}$$

where C_{jbs} is the unit-area bottom S/B junciton capacitance, C_{jbssw} is the unit-length S/B junction sidewall capacitance along the isolation edge, and C_{jbsswg} is the unit-length S/B junction sidewall capacitance along the gate edge. The effective area and perimeters in (10.2.1) are given in Chapter 11.

C_{jbs} is calculated by

if $V_{bs} < 0$

$$C_{jbs} = CJS(T) \cdot \left(1 - \frac{V_{bs}}{PBS(T)}\right)^{-MJS} \tag{10.2.2}$$

otherwise

(10.2.3)

$$C_{jbs} = CJS(T) \cdot \left(1 + MJS \cdot \frac{V_{bs}}{PBS(T)} \right)$$

C_{jbssw} is calculated by

if $V_{bs} < 0$

(10.2.4)

$$C_{jbssw} = CJSWS(T) \cdot \left(1 - \frac{V_{bs}}{PBSWS(T)} \right)^{-MJSWS}$$

otherwise

(10.2.5)

$$C_{jbssw} = CJSWS(T) \cdot \left(1 + MJSWS \cdot \frac{V_{bs}}{PBSWS(T)} \right)$$

C_{jbsswg} is calculated by

if $V_{bs} < 0$

(10.2.6)

$$C_{jbsswg} = CJSWGS(T) \cdot \left(1 - \frac{V_{bs}}{PBSWGS(T)} \right)^{-MJSWGS}$$

otherwise

(10.2.7)

$$C_{jbsswg} = CJSWGS(T)\cdot\left(1-\frac{V_{bs}}{PBSWGS(T)}\right)^{-MJSWGS}$$

10.2.2 Drain/Body Junction Diode

The drain-side junction capacitance can be calculated by

(10.2.8)

$$C_{bd} = A_{deff}C_{jbd} + P_{deff}C_{jbdsw} + W_{effcj}\cdot NF\cdot C_{jbdswg}$$

where C_{jbd} is the unit-area bottom D/B junciton capacitance, C_{jbdsw} is the unit-length D/B junction sidewall capacitance along the isolation edge, and C_{jbdswg} is the unit-length D/B junction sidewall capacitance along the gate edge. The effective area and perimeters in (10.2.8) are given in Chapter 11.

C_{jbd} is calculated by

if $V_{bd} < 0$

(10.2.9)

$$C_{jbd} = CJD(T)\cdot\left(1-\frac{V_{bd}}{PBD(T)}\right)^{-MJD}$$

otherwise

(10.2.10)

$$C_{jbd} = CJD(T)\cdot\left(1+MJD\cdot\frac{V_{bd}}{PBD(T)}\right)$$

C_{jbdsw} is calculated by

if $V_{bd} < 0$

(10.2.11)

$$C_{jbdsw} = CJSWD(T) \cdot \left(1 - \frac{V_{bd}}{PBSWD(T)}\right)^{-MJSWD}$$

otherwise

(10.2.12)

$$C_{jbdsw} = CJSWD(T) \cdot \left(1 + MJSWD \cdot \frac{V_{bd}}{PBSWD(T)}\right)$$

C_{jbdswg} is calculated by

if $V_{bd} < 0$

(10.2.13)

$$C_{jbdswg} = CJSWGD(T) \cdot \left(1 - \frac{V_{bd}}{PBSWGD(T)}\right)^{-MJSWGD}$$

otherwise

(10.2.14)

$$C_{jbdswg} = CJSWGD(T) \cdot \left(1 + MJSWGD \cdot \frac{V_{bd}}{PBSWGD(T)}\right)$$