Chapter 5: Drain Current Model

5.1 Bulk Charge Effect

The depletion width will not be uniform along channel when a non-zero V_{ds} is applied. This will cause V_{th} to vary along the channel. This effect is called bulk charge effect.

BSIM4 uses A_{bulk} to model the bulk charge effect. Several model parameters are introduced to account for the channel length and width dependences and bias effects. A_{bulk} is formulated by

(5.1.1)

$$A_{bulk} = \left\{1 + F\_doping \cdot \left[\left(1 - AGS \cdot V_{gsteff}\left(\frac{L_{eff}}{L_{eff} + 2\sqrt{XJ \cdot X_{dep}}}\right)^2\right) + \frac{B0}{W_{eff}' + B1}\right] \cdot \frac{A0 \cdot L_{eff}}{L_{eff} + 2\sqrt{XJ \cdot X_{dep}}}\right\} \cdot \frac{1}{1 + KETA \cdot V_{bseff}}$$

where the second term on the RHS is used to model the effect of non-uniform doping profiles

(5.1.2)

$$F\_doping = \frac{\sqrt{1 + LPEB / L_{eff}}\, K_{1ox}}{2\sqrt{\Phi_s - V_{bseff}}} + K_{2ox} - K3B \frac{TOXE}{W_{eff}' + W0} \Phi_s$$

Note that A_{bulk} is close to unity if the channel length is small and increases as the channel length increases.

5.2 Unified Mobility Model

A good mobility model is critical to the accuracy of a MOSFET model. The scattering mechanisms responsible for surface mobility basically include phonons, coulombic scattering, and surface roughness. For good quality interfaces, phonon scattering is generally the dominant scattering mechanism at room temperature. In general, mobility depends on many process parameters and bias conditions. For example, mobility depends on the gate oxide thickness, substrate doping concentration, threshold voltage, gate and substrate voltages, etc. [5] proposed an empirical unified formulation based on the concept of an effective field E_{eff} which lumps many process parameters and bias conditions together. E_{eff} is defined by

$$E_{eff} = \frac{Q_B + (Q_n/2)}{e_{si}} \tag{5.2.1}$$

The physical meaning of E_{eff} can be interpreted as the average electric field experienced by the carriers in the inversion layer. The unified formulation of mobility is then given by

$$m_{eff} = \frac{m_0}{1 + (E_{eff} \big/ E_0)^n} \tag{5.2.2}$$

For an NMOS transistor with n-type poly-silicon gate, (5.2.1) can be rewritten in a more useful form that explicitly relates E_{eff} to the device parameters

(5.2.3)

$$E_{eff} \approx \frac{V_{gs} + V_{th}}{6TOXE}$$

BSIM4 provides three different models of the effective mobility. The ***mobMod*** = 0 and 1 models are from BSIM3v3.2.2; the new ***mobMod*** = 2, a universal mobility model, is more accurate and suitable for predictive modeling.

- ***mobMod* = 0**

(5.2.4)

$$\mu_{eff} = \frac{U0}{1 + \left(UA + UCV_{bseff}\right)\left(\frac{V_{gsteff} + 2V_{th}}{TOXE}\right) + UB\left(\frac{V_{gsteff} + 2V_{th}}{TOXE}\right)^2}$$

- ***mobMod* = 1**

(5.2.5)

$$\mu_{eff} = \frac{U0}{1 + \left[UA\left(\frac{V_{gsteff} + 2V_{th}}{TOXE}\right) + UB\left(\frac{V_{gsteff} + 2V_{th}}{TOXE}\right)^2\right]\left(1 + UC \cdot V_{bseff}\right)}$$

- ***mobMod* = 2**

(5.2.6)

$$\mu_{eff} = \frac{U0}{1 + \left(UA + UC \cdot V_{bseff}\right)\left[\frac{V_{gsteff} + C_0 \cdot \left(VTHO - VFB - \Phi_s\right)}{TOXE}\right]^{EU}}$$

where the constant C_0 = 2 for NMOS and 2.5 for PMOS.

5.3 Asymmetric and Bias-Dependent Source/ Drain Resistance Model

BSIM4 models source/drain resistances in two components: bias-independent diffusion resistance (sheet resistance) and bias-dependent LDD resistance. Accurate modeling of the bias-dependent LDD resistances is important for deep-submicron CMOS technologies. In BSIM3 models, the LDD source/drain resistance R_{ds}(V) is modeled internally through the I-V equation and symmetry is assumed for the source and drain sides. BSIM4 keeps this option for the sake of simulation efficiency. In addition, BSIM4 allows the source LDD resistance R_s(V) and the drain LDD resistance R_d(V) to be external and asymmetric (i.e. R_s(V) and R_d(V) can be connected between the external and internal source and drain nodes, respectively; furthermore, R_s(V) does not have to be equal to R_d(V)). This feature makes accurate RF CMOS simulation possible. The internal R_{ds}(V) option can be invoked by setting the model selector ***rdsMod*** = 0 (**interna**l) and the external one for R_s(V) and R_d(V) by setting ***rdsMod*** = 1 (**external**).

- ***rdsMod*** = 0 (Internal R_{ds}(V))

(5.3.1)

$$R_{ds}(V) = \left\{ \begin{array}{l} RDSWMIN + RDSW \cdot \\ \left[PRWB \cdot \left(\sqrt{\Phi_s - V_{bseff}} - \sqrt{\Phi_s} \right) + \dfrac{1}{1 + PRWG \cdot V_{gsteff}} \right] \end{array} \right\} \Bigg/ \left(1e6 \cdot W_{effcj} \right)^{WR}$$

- ***rdsMod*** = 1 (External R_d(V) and R_s(V))

(5.3.2)

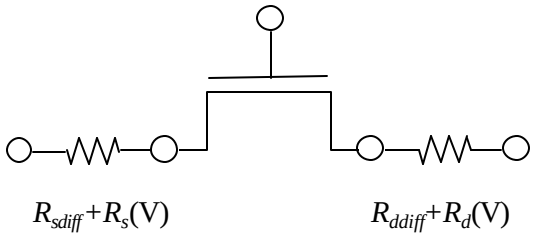
$$R_d(V) = \left\{ \begin{array}{l} RDWMIN + RDW \cdot \\ \left[-PRWB \cdot V_{bd} + \dfrac{1}{1 + PRWG \cdot \left(V_{gd} - V_{fbsd} \right)} \right] \end{array} \right\} \Bigg/ \left[\left(1e6 \cdot W_{effcj} \right)^{WR} \cdot NF \right]$$

(5.3.3)

$$R_s(V)=\left\{\begin{bmatrix} RSWMIN + RSW \cdot \\ \left[-PRWB \cdot V_{bs} + \frac{1}{1+PRWG\cdot(V_{gs}-V_{fbsd})}\right] \end{bmatrix}\right\} \Big/ \left[(1e6\cdot W_{effcj})^{WR}\cdot NF\right]$$

V_{fbsd} is the calculated flat-band voltage between gate and source/drain as given in Section 4.3.2.

The following figure shows the schematic of source/drain resistance connection for ***rdsMod*** = 1.



The diffusion source/drain resistance R_{sdiff} and R_{ddiff} models are given in the chapter of layout-dependence models.

5.4 Drain Current for Triode Region

5.4.1 $R_{ds}(V)$=0 or *rdsMod*=1 (“intrinsic case”)

Both drift and diffusion currents can be modeled by

(5.4.1)

$$I_{ds}(y) = WQ_{ch}(y)\mu_{ne}(y)\frac{dV_F(y)}{dy}$$

where $u_{ne}(y)$ can be written as

(5.4.2)

$$\mu_{ne(y)} = \frac{\mu_{eff}}{1+\frac{E_y}{E_{sat}}}$$

Substituting (5.4.2) in (5.4.1), we get

(5.4.3)

$$I_{ds}(y) = WQ_{ch0}\left(1-\frac{V_F(y)}{V_b}\right)\frac{\mu_{eff}}{1+\frac{E_y}{E_{sat}}}\frac{dV_F(y)}{dy}$$

(5.4.3) is integrated from source to drain to get the expression for linear drain current. This expression is valid from the subthreshold regime to the strong inversion regime

(5.4.4)

$$I_{ds0} = \frac{W\mu_{eff}Q_{ch0}V_{ds}\left(1-\frac{V_{ds}}{2V_b}\right)}{L\left(1+\frac{V_{ds}}{E_{sat}L}\right)}$$

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5.4.2 R_{ds}(V) > 0 and *rdsMod*=0 ("Extrinsic case")

The drain current in this case is expressed by

(5.4.5)

$$I_{ds} = \frac{I_{dso}}{1 + \frac{R_{ds} I_{dso}}{V_{ds}}}$$

5.5 Velocity Saturation

Velocity saturation is modeled by [5]

(5.5.1)

$$v = \frac{m_{eff} E}{1 + E/E_{sat}} \quad E < E_{sat}$$
$$= VSAT \qquad E \geq E_{sat}$$

where E_{sat} corresponds to the critical electrical field at which the carrier velocity becomes saturated. In order to have a continuous velocity model at $E = E_{sat}$, E_{sat} must satisfy

(5.5.2)

$$E_{sat} = \frac{2VSAT}{m_{eff}}$$

5.6 Saturation Voltage V_{dsat}

5.6.1 Intrinsic case

In this case, the LDD source/drain resistances are either zero or non zero but not modeled inside the intrinsic channel region. It is easy to obtain V_{dsat} as [7]

$$V_{dsat} = \frac{E_{sat}L(V_{gsteff} + 2v_t)}{A_{bulk}E_{sat}L + V_{gsteff} + 2v_t} \tag{5.6.1}$$

5.6.2 Extrinsic Case

In this case, non-zero LDD source/drain resistance R_{ds}(V) is modeled internally through the I-V equation and symetry is assumed for the source and drain sides. V_{dsat} is obtained as [7]

$$V_{dsat} = \frac{-b - \sqrt{b^2 - 4ac}}{2a} \tag{5.6.2a}$$

where

$$a = A_{bulk}{}^2 W_{eff} VSATC_{oxe} R_{ds} + A_{bulk}\left(\frac{1}{l} - 1\right) \tag{5.6.2b}$$

(5.6.2c)

$$b = -\begin{bmatrix} (V_{gsteff} + 2v_t)\left(\frac{2}{l} - 1\right) + A_{bulk}E_{sat}L_{eff} \\ + 3A_{bulk}(V_{gsteff} + 2v_t)W_{eff}VSATC_{oxe}R_{ds} \end{bmatrix}$$

(5.6.2d)

$$c = (V_{gsteff} + 2v_t)E_{sat}L_{eff} + 2(V_{gsteff} + 2v_t)^2 W_{eff}VSATC_{oxe}R_{ds}$$

(5.6.2e)

$$l = A1V_{gsteff} + A2$$

λ is introduced to model the non-saturation effects which are found for PMOSFETs.

5.6.3 V_{dseff} Formulation

An effective V_{ds}, V_{dseff}, is used to ensure a smooth transition near V_{dsat} from trode to saturation regions. V_{dseff} is formulated as

(5.6.3)

$$V_{dseff} = V_{dsat} - \frac{1}{2}\left[(V_{dsat} - V_{ds} - d) + \sqrt{(V_{dsat} - V_{ds} - d)^2 + 4d \cdot V_{dsat}}\right]$$

where δ (*DELTA*) is a model parameter.

5.7 Saturation-Region Output Conductance Model

A typical I-V curve and its output resistance are shown in Figure 5-1. Considering only the channel current, the I-V curve can be divided into two parts: the linear region in which the current increases quickly with the drain voltage and the saturation region in which the drain current has a weaker dependence on the drain voltage. The first order derivative reveals more detailed information about the physical mechanisms which are involved in the device operation. The output resistance curve can be divided into four regions with distinct R_{out}~V_{ds} dependences.

The first region is the triode (or linear) region in which carrier velocity is not saturated. The output resistance is very small because the drain current has a strong dependence on the drain voltage. The other three regions belong to the saturation region. As will be discussed later, there are several physical mechanisms which affect the output resistance in the saturation region: channel length modulation (CLM), drain-induced barrier lowering (DIBL), and the substrate current induced body effect (SCBE). These mechanisms all affect the output resistance in the saturation range, but each of them dominates in a specific region. It will be shown

next that CLM dominates in the second region, DIBL in the third region, and SCBE in the fourth region.

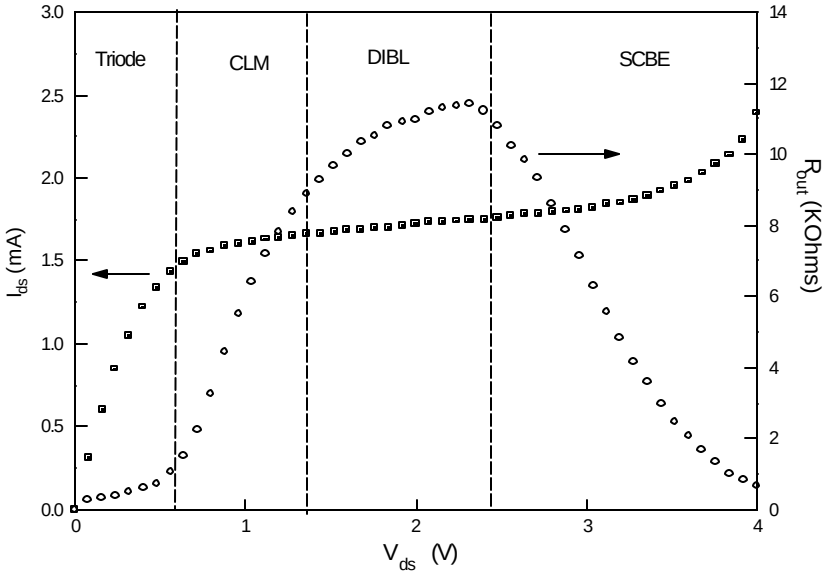

Figure 5-1. General behavior of MOSFET output resistance.

The channel current is a function of the gate and drain voltage. But the current depends on the drain voltage weakly in the saturation region. In the following, the Early voltage is introduced for the analysis of the output resistance in the saturation region:

(5.7.1)

$$I_{ds}(V_{gs},V_{ds}) = I_{dsat}(V_{gs},V_{dsat}) + \int_{V_{dsat}}^{V_{ds}} \frac{\partial I_{ds}(V_{gs},V_{ds})}{\partial V_d} \cdot dV_d$$

$$= I_{dsat}(V_{gs},V_{dsat}) \cdot \left[1 + \int_{V_{dsat}}^{V_{ds}} \frac{1}{V_A} \cdot dV_d \right]$$

where the Early voltage V_A is defined as

(5.7.2)

$$V_A = I_{dsat} \cdot \left[\frac{\partial I_{ds}(V_{gs}, V_{ds})}{\partial V_d} \right]^{-1}$$

We assume in the following analysis that the contributions to the Early voltage from all mechanisms are independent and can be calculated separately.

5.7.1 Channel Length Modulation (CLM)

If channel length modulation is the only physical mechanism to be taken into account, the Early voltage can be calculated by

(5.7.3)

$$V_{ACLM} = I_{dsat} \cdot \left[\frac{\partial I_{ds}(V_{gs}, V_{ds})}{\partial L} \cdot \frac{\partial L}{\partial V_d} \right]^{-1}$$

Based on quasi two-dimensional analysis and through integration, we propose V_{ACLM} to be

(5.7.4)

$$V_{ACLM} = C_{clm} \cdot (V_{ds} - V_{dsat})$$

where

(5.7.5)

$$C_{clm} = \frac{1}{PCLM} \cdot F \cdot \left(1 + PVAG \frac{V_{gsteff}}{E_{sat} L_{eff}} \right) \left(1 + \frac{R_{ds} \cdot I_{dso}}{V_{dseff}} \right) \left(L_{eff} + \frac{V_{dsat}}{E_{sat}} \right) \cdot \frac{1}{litl}$$

and the *F* factor to account for the impact of pocket implant technology is

(5.7.6)

$$F = \frac{1}{1 + FPROUT \cdot \frac{\sqrt{L_{eff}}}{V_{gsteff} + 2v_t}}$$

and *litl* in (5.7.5) is given by

(5.7.7)

$$litl = \sqrt{\frac{e_{si} TOXE \cdot XJ}{EPSROX}}$$

PCLM is introduced into V_{ACLM} to compensate for the error caused by *XJ* since the junction depth *XJ* can not be determined very accurately.

5.7.2 Drain-Induced Barrier Lowering (DIBL)

The Early voltage V_{ADIBLC} due to DIBL is defined as

(5.7.8)

$$V_{ADIBL} = I_{dsat} \cdot \left[\frac{\partial I_{ds}(V_{gs}, V_{ds})}{\partial V_{th}} \cdot \frac{\partial V_{th}}{\partial V_d} \right]^{-1}$$

V_{th} has a linear dependence on V_{ds}. As channel length decreases, V_{ADIBLC} decreases very quickly

(5.7.9)

$$V_{ADIBL} = \frac{V_{gsteff} + 2v_t}{q_{rout}(1 + PDIBLCB \cdot V_{bseff})} \left(1 - \frac{A_{bulk} V_{dsat}}{A_{bulk} V_{dsat} + V_{gsteff} + 2v_t} \right) \cdot \left(1 + PVAG \frac{V_{gsteff}}{E_{sat} L_{eff}} \right)$$

where q_{rout} has a similar dependence on the channel length as the DIBL effect in V_{th}, but a separate set of parameters are used:

$$q_{rout} = \frac{PDIBLC1}{2\cosh\left(\frac{DROUT \cdot L_{eff}}{lt0}\right) - 2} + PDIBLC2 \tag{5.7.10}$$

Parameters *PDIBLC*1, *PDIBLC*2, *PDIBLCB* and *DROUT* are introduced to correct the DIBL effect in the strong inversion region. The reason why *DVT*0 is not equal to *PDIBLC*1 and *DVT*1 is not equal to *DROUT* is because the gate voltage modulates the DIBL effect. When the threshold voltage is determined, the gate voltage is equal to the threshold voltage. But in the saturation region where the output resistance is modeled, the gate voltage is much larger than the threshold voltage. Drain induced barrier lowering may not be the same at different gate bias. *PDIBLC*2 is usually very small. If *PDIBLC*2 is put into the threshold voltage model, it will not cause any significant change. However it is an important parameter in V_{ADIBLC} for long channel devices, because *PDIBLC*2 will be dominant if the channel is long.

5.7.3 Substrate Current Induced Body Effect (SCBE)

When the electrical field near the drain is very large (> 0.1MV/cm), some electrons coming from the source (in the case of NMOSFETs) will be energetic (hot) enough to cause impact ionization. This will generate electron-hole pairs when these energetic electrons collide with silicon atoms. The substrate current I_{sub} thus created during impact ionization will

increase exponentially with the drain voltage. A well known I_{sub} model [8] is

$$I_{sub} = \frac{A_i}{B_i} I_{ds}(V_{ds} - V_{dsat}) \exp\left(-\frac{B_i \cdot litl}{V_{ds} - V_{dsat}}\right) \tag{5.7.11}$$

Parameters A_i and B_i are determined from measurement. I_{sub} affects the drain current in two ways. The total drain current will change because it is the sum of the channel current as well as the substrate current. The total drain current can now be expressed as follows

$$I_{ds} = I_{ds-w/o-Isub} + I_{sub} = I_{ds-w/o-Isub} \cdot \left[1 + \frac{V_{ds} - V_{dsat}}{\frac{B_i}{A_i} \exp\left(\frac{B_i \cdot litl}{V_{ds} - V_{dsat}}\right)}\right] \tag{5.7.12}$$

The Early voltage due to the substrate current V_{ASCBE} can therefore be calculated by

$$V_{ASCBE} = \frac{B_i}{A_i} \exp\left(\frac{B_i \cdot litl}{V_{ds} - V_{dsat}}\right) \tag{5.7.13}$$

We can see that V_{ASCBE} is a strong function of V_{ds}. In addition, we also observe that V_{ASCBE} is small only when V_{ds} is large. This is why SCBE is important for devices with high drain voltage bias. The channel length and gate oxide dependence of V_{ASCBE} comes from V_{dsat} and *litl*. We replace B_i with *PSCBE*2 and A_i/B_i with $PSCBE1/L_{eff}$ to get the following expression for V_{ASCBE}

(5.7.14)

$$\frac{1}{V_{ASCBE}} = \frac{PSCBE2}{L_{eff}} \exp\left(-\frac{PSCBE1 \cdot litl}{V_{ds} - V_{dsat}}\right)$$

5.7.4 Drain-Induced Threshold Shift (DITS) by Pocket Implant

It has been shown that a long-channel device with pocket implant has a smaller R_{out} than that of uniformly-doped device [3]. The R_{out} degradation factor F is given in (5.7.6). In addition, the pocket implant introduces a potential barrier at the drain end of the channel. This barrier can be lowered by the drain bias even in long-channel devices. The Early voltage due to DITS is modeled by

(5.7.15)

$$V_{ADITS} = \frac{1}{PDITS} \cdot F \cdot \left[1 + \left(1 + PDITSL \cdot L_{eff}\right) \exp\left(PDITSD \cdot V_{ds}\right)\right]$$

5.8 Single-Equation Channel Current Model

The final channel current equation for both linear and saturation regions now becomes

(5.8.1)

$$I_{ds} = \frac{I_{ds0} \cdot NF}{1 + \frac{R_{ds} I_{ds0}}{V_{dseff}}} \left[1 + \frac{1}{C_{clm}} \ln\left(\frac{V_A}{V_{Asat}}\right)\right] \cdot \left(1 + \frac{V_{ds} - V_{dseff}}{V_{ADIBL}}\right) \cdot \left(1 + \frac{V_{ds} - V_{dseff}}{V_{ADITS}}\right) \cdot \left(1 + \frac{V_{ds} - V_{dseff}}{V_{ASCBE}}\right)$$

where NF is the number of device fingers, and

(5.8.2)

V_A is written as

(5.8.3)

$$V_A = V_{Asat} + V_{ACLM}$$

where V_{Asat} is

(5.8.4)

$$V_{Asat} = \frac{E_{sat}L_{eff} + V_{dsat} + 2R_{ds}vsatC_{oxe}W_{eff}V_{gsteff} \cdot \left[1 - \frac{A_{bulk}V_{dsat}}{2\left(V_{gsteff} + 2v_t\right)}\right]}{R_{ds}vsatC_{oxe}W_{eff}A_{bulk} - 1 + \frac{2}{l}}$$

V_{Asat} is the Early voltage at $V_{ds} = V_{dsat}$. V_{Asat} is needed to have continuous drain current and output resistance expressions at the transition point between linear and saturation regions.